

WHAT IS CLAIMED IS:

1 1. A high speed adder in which provisional carriers
 2 composed of a pair of signals that indicate a case where carry
 3 is produced from a low order bit and a case where no carry is
 4 produced therefrom are generated in advance and an actual carrier
 5 is selected from the provisional carriers in accordance with
 6 selection information from the low order bit:

7 a carrier transfer path; and

8 a plurality of converters, each of which converts the
 9 provisional carriers into provisional sums composed of a pair
 10 of signals that indicate the case where the carry is produced
 11 from the low order bit and the case where no carry is produced
 12 therefrom, the converters being provided on a predetermined
 13 portion of the carrier transfer path.

1 2. An adder according to claim 1, wherein, when the adder
 2 is a 2^N (N is an integer of 3 or more)-bit adder, the carrier
 3 transfer path comprises $(N+1)$ or less circuit stages,

4 wherein a first circuit stage receives two input data for
 5 each corresponding bit and an input carry signal from an outside,
 6 generates a bit sum of a least significant bit, outputs the bit
 7 sum to the outside, generates provisional carriers corresponding
 8 to each of bits other than the least significant bit, and outputs
 9 the generated provisional carriers to a following circuit stage,

10 wherein second to N -th circuit stages convert the
 11 provisional carriers corresponding to higher $(2^{(N-1)}-1)$ bits
 12 other than a most significant bit, of the provisional carriers
 13 into the provisional sums by at least one of the converters in
 14 course of transfer, and generate actual carriers from the
 15 provisional carriers corresponding to lower $(2^{(N-1)}-1)$ bits other

16 than the least significant bit, and
17 wherein a $(N+1)$ -th circuit stage outputs data other than
18 a bit sum of the least significant bit, of sum data of the two
19 input data and an output carry signal to the outside.

1 3. An adder according to claim 2, wherein, when the input
2 data is arranged in an order from the most significant bit to
3 the least significant bit, at least one of the converters is
4 located corresponding to a $(2^{(N-M-1)}+1)$ -th bit to a $2^{(N-M)}$ -th bit
5 from the most significant bit of the input data in a $(N-M+1)$ -th
6 circuit stage which is specified by an integer M that satisfies
7 $1 \leq M < N$.

1 4. An adder according to claim 2, wherein the first circuit
2 stage comprises:
3 (2^N-1) conditional cells, each of which receives
4 corresponding bits of the two input data to perform an exclusive
5 OR operation, generates the provisional carriers composed of
6 the pair of signals that indicate the case where the carry is
7 produced from the low order bit and the case where no carry is
8 produced therefrom, and outputs the generated provisional
9 carriers, the conditional cells being provided corresponding
10 to a most significant bit of 2^N bits to a bit higher than the
11 least significant bit thereof by one; and
12 a full adder that receives the least significant bits of
13 the two input data and the output carry signal and generates
14 an exclusive OR signal and a carry signal.

1 5. An adder according to claim 4, wherein each of the
2 conditional cells comprises:

3 a first gate that receives two input bits and performs
 4 an AND operation on the two input bits to output a first signal;
 5 a second gate that receives the two input bits and performs
 6 an OR operation on the two input bits to output a second signal;
 7 a third gate that receives the first signal outputted from
 8 the first gate and inverts the received first signal to output
 9 a third signal; and
 10 a fourth gate that receives the second signal outputted
 11 from the second gate and the third signal outputted from the
 12 third gate and performs the AND operation on the second signal
 13 and the third signal to output a fourth signal,
 14 wherein the first signal outputted from the first gate
 15 is given as a first carry signal which is the carry signal in
 16 the case where no carry is produced from the low order bit,
 17 wherein the second signal outputted from the second gate
 18 is given as a second carry signal which is the carry signal in
 19 the case where the carry is produced from the low order bit,
 20 and
 21 wherein the fourth signal outputted from the fourth gate
 22 is a result of the exclusive OR operation performed on the two
 23 input bits.

1 6. An adder according to claim 4, wherein, of the circuit
 2 stages, when the $(N-M+1)$ -th circuit stage which is specified
 3 by the integer M that satisfies $1 \leq M < N$ is divided in a virtual
 4 form into 2^M sub-circuits corresponding to every $2^{(N-M)}$ bits of
 5 the input data,
 6 the $(N-M+1)$ -th circuit stage comprises:
 7 $2^{(N-M-1)}$ multiplexers, each of which receives a pair of
 8 signals which are outputs of one of the conditional cell and

9 the carry selector which are provided for a corresponding bit
 10 in a preceding circuit stage; receives a signal outputted from
 11 one of the full adder and the multiplexer which are provided
 12 for a bit in a circuit stage preceding by one stage, and which
 13 corresponds to a $(2^{(N-M-1)}+1)$ -th bit from a top in a first
 14 sub-arithmetic circuit; selects an actual carry signal in
 15 accordance with the received signal; and outputs the actual carry
 16 signal, the multiplexers being provided corresponding to higher
 17 $2^{(N-M-1)}$ bits of the first sub-arithmetic circuit which include
 18 an input from a bit corresponding to a $2^{(N-M)}$ -th bit from the
 19 least significant bit in a high order direction;

20 $(2^{(N-1)} - 2^{(N-M-1)})$ carry selectors, each of which receives
 21 a pair of signals which are outputs of one of the conditional
 22 cell, the carry selector, and the converter, which are provided
 23 for the corresponding bit in the preceding circuit stage;
 24 receives a pair of selection signals which are outputs of one
 25 of the conditional cell and the carry selector which are provided
 26 for a bit in the circuit stage preceding by one stage, and which
 27 corresponds to the $(2^{(N-M-1)}+1)$ -th bit from the top in a
 28 sub-circuit; selects a pair of signals indicating the provisional
 29 carriers or the provisional sums in the following circuit stage
 30 in accordance with the selection signals; and outputs the
 31 selected pair of signals, the carry selectors being provided
 32 corresponding to the higher $2^{(N-M-1)}$ bits in the sub-circuit which
 33 is included in a second sub-arithmetic circuit composed of a
 34 sub-circuit that receives a carry signal corresponding to the
 35 most significant bit or a third sub-arithmetic circuit composed
 36 of second to (2^M-1) -th sub-circuits from the second
 37 sub-arithmetic circuit in the low order direction; and

38 $2^{(N-M-1)}$ converters, each of which receives a pair of signals

39 which are outputs of one of the conditional cell and the carry
40 selector which are provided for the corresponding bit in the
41 preceding circuit stage and indicate the provisional carriers,
42 and an exclusive OR signal outputted from the conditional cell
43 corresponding to a bit higher by one bit in the first circuit
44 stage; converts the received pair of signals into a pair of signals
45 indicating the provisional sums; and outputs the pair of signals
46 indicating the provisional sums, the converters being provided
47 corresponding to lower $2^{(N-M-1)}$ bits in the second sub-arithmetic
48 circuit.

1 7. An adder according to claim 6, wherein each of the
2 conditional cells comprises:

3 a first gate that receives two input bits and performs
4 an AND operation on the two input bits to output a first signal;

5 a second gate that receives the two input bits and performs
6 an OR operation on the two input bits to output a second signal;

7 a third gate that receives the first signal outputted from
8 the first gate and inverts the received first signal to output
9 a third signal; and

10 a fourth gate that receives the second signal outputted
11 from the second gate and the third signal outputted from the
12 third gate and performs an AND operation on the second signal
13 and the third signal to output a fourth signal,

14 wherein the first signal outputted from the first gate
15 is given as a first carry signal which is the carry signal in
16 the case where no carry is produced from the low order bit,

17 wherein the second signal outputted from the second gate
18 is given as a second carry signal which is the carry signal in
19 the case where the carry is produced from the low order bit,

20 and

21 wherein the fourth signal outputted from the fourth gate
22 is a result of the exclusive OR operation performed on the two
23 input bits.

1 8. An adder according to claim 6, wherein each of the
2 converters comprises:

3 a first exclusive OR circuit that receives one of the pair
4 of signals indicating the provisional carriers and the exclusive
5 OR signal outputted from the conditional cell corresponding to
6 the bit higher by one bit in the first circuit stage and outputs
7 one of the pair of signals indicating the provisional sums; and
8 a second exclusive OR circuit that receives the other of
9 the pair of signals indicating the provisional carriers and the
10 exclusive OR signal, and outputs the other of the pair of signals
11 indicating the provisional sums.

1 9. An adder according to claim 6, wherein each of the carry
2 selectors comprises:

3 a first multiplexer that receives a pair of input signals
4 indicating the provisional carriers, selects one of the pair
5 of input signals in accordance with one of the pair of selection
6 signals, and outputs the selected one as one of a pair of output
7 signals; and

8 a second multiplexer that receives the pair of input
9 signals, selects one of the pair of input signals in accordance
10 with the other of the pair of selection signals, and outputs
11 the selected one as the other of the pair of output signals.

1 10. An adder according to claim 6, wherein the (N+1)-th

2 circuit stage comprises:

3 a multiplexer that receives a pair of signals outputted
4 from a highest order carry selector provided corresponding to
5 the most significant bit of the input data in the N-th circuit
6 stage, selects an output carry signal in accordance with the
7 selection signal outputted the multiplexer corresponding to a
8 $(2^{(N-1)}+1)$ -th bit from the most significant bit of the input data
9 in the low order direction in the N-th circuit stage, and outputs
10 the output carry signal;

11 $(2^{(N-1)}-1)$ multiplexers, each of which receives the pair
12 of signals outputted from one of the carry selector and the
13 converter which are provided for a corresponding bit in the N-th
14 circuit stage, selects a signal corresponding to an actual bit
15 sum of a bit higher by one bit in accordance with the selection
16 signal outputted from the multiplexer corresponding to the
17 $(2^{(N-1)}+1)$ -th bit from the most significant bit of the input data
18 in the low order direction in the N-th circuit stage, and outputs
19 the signal corresponding to an actual bit sum of a bit higher
20 by one bit, the multiplexers being provided corresponding to
21 a second bit to a $2^{(N-1)}$ -th bit from the most significant bit
22 of the input data in the low order direction; and

23 $2^{(N-1)}$ exclusive OR circuits, each of which receives the
24 actual carry signal outputted from one of the full adder and
25 the multiplexer which are provided for the corresponding bit
26 in a preceding circuit stage and the exclusive OR signal outputted
27 from the conditional cell corresponding to the bit higher by
28 one bit in the first circuit stage, and outputs a signal
29 corresponding to an actual bit sum of a bit higher by one bit,
30 the exclusive OR circuits being provided corresponding to a
31 $(2^{(N-1)}+1)$ -th bit to a 2^N -th bit from the most significant bit

32 of the input data in the low order direction.

1 11. An adder according to claim 10, wherein each of the
2 conditional cells comprises:

3 a first gate that receives two input bits and performs
4 an AND operation on the two input bits to output a first signal;

5 a second gate that receives the two input bits and performs
6 an OR operation on the two input bits to output a second signal;

7 a third gate that receives the first signal outputted from
8 the first gate and inverts the received first signal to output
9 a third signal; and

10 a fourth gate that receives the second signal outputted
11 from the second gate and the third signal outputted from the
12 third gate and performs the AND operation on the second signal
13 and the third signal to output a fourth signal,

14 wherein the first signal outputted from the first gate
15 is given as a first carry signal which is the carry signal in
16 the case where no carry is produced from the low order bit,

17 wherein the second signal outputted from the second gate
18 is given as a second carry signal which is the carry signal in
19 the case where the carry is produced from the low order bit,
20 and

21 wherein the fourth signal outputted from the fourth gate
22 is a result of the exclusive OR operation on the two input bits.

1 12. An adder according to claim 10, wherein each of the
2 converters comprises:

3 a first exclusive OR circuit that receives one of the pair
4 of signals indicating the provisional carriers and the exclusive
5 OR signal outputted from the conditional cell corresponding to

6 the bit higher by one bit in the first circuit stage, and outputs
7 one of the pair of signals indicating the provisional sums; and
8 a second exclusive OR circuit that receives the other of
9 the pair of signals indicating the provisional carriers and the
10 exclusive OR signal, and outputs the other of the pair of signals
11 indicating the provisional sums.

1 13. An adder according to claim 10, wherein each of the
2 carry selectors comprises:
3 a first multiplexer that receives a pair of input signals
4 indicating the provisional carriers, selects one of the pair
5 of input signals in accordance with one of the pair of selection
6 signals, and outputs the selected one as one of a pair of output
7 signals; and
8 a second multiplexer that receives the pair of input
9 signals, selects one of the pair of input signals in accordance
10 with the other of the pair of selection signals, and outputs
11 the selected one as the other of the pair of output signals.